IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application:	G.R. Mohan Rao
Serial No.:	10/665,906
Filed:	September 18, 2003
Art Unit:	2188
Examiner:	Portka, Gary J.
Title:	MEMORIES FOR ELECTRONIC SYSTEMS

REPLY BRIEF UNDER 37 C.F.R. §41.41

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is being submitted in response to the Examiner's Answer dated February 20, 2007, with a two-month statutory period for response set to expire on April 20, 2007.

I. RESPONSE TO EXAMINER'S ARGUMENTS:

A. Response to Examiner's assertion that claims 1-21 are properly rejected under 35 U.S.C. §112, second paragraph, as discussed on pages 8-9 of Examiner's Answer.

The Examiner states:

> Appellant's response to the 35 USC 112 second paragraph rejection (pages 4-7 of the brief) simply cites the specification, but the cited sections do not clarify these limitations of the claims (in light of related assertions by Appellant that the references do not disclose them), and so the rejection is maintained hereinabove. That is, it is not apparent why two identical adjacent columns may not be considered as combined into a single column, absent any further defining characteristics of a 'single column' other than a vertical arrangement of elements. Also, it is not apparent that when rows of the references are transferred in a single operation, why those rows might not be properly considered of a 'predetermined word-width', absent any further defining characteristics of a 'predetermined word-width' other than a data length handled in a single operation. Examiner's Answer, pages 8-9.

As best understood by Appellant, the Examiner appears to believe that is appropriate to reject claims 1-21 under 35 U.S.C. §112, second paragraph, because Appellant did not point to a particular sentence in Appellant's Specification that specifically states that a single column cannot be considered as two identical adjacent columns. First, Appellant is not required to address every possible unreasonable interpretation of a word or phrase in their Specification. It is impossible to know what unreasonable interpretation of a word or phrase may be made. That is why the Examiner is required to provide a basis in fact and/or technical reasoning for asserting that when Appellant describes an array of memory cells as including a single column that this single column must somehow be comprised of smaller columns. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that when Appellant describes an array of memory cells as including a single column that this single column must somehow be comprised of smaller columns, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999).

Further, not defining a term in the claims or in the Specification is not by itself sufficient grounds for rejecting those claims under 35 U.S.C. §112, second paragraph.

A claim term that is not used or defined in the Specification is not indefinite if the meaning of the claim term is discernible. *Bancorp Services, L.L.C. v. Hartford Life Ins. Co.*, 359 F.3d 1367, 1372, 69 U.S.P.Q.2d 1996, 1999-2000 (Fed. Cir. 2000). As shown in Appellant's Second Appeal Brief (pages 4-7), the meaning of claims 1-21 is discernible and hence claims 1-21 are allowable under 35 U.S.C. §112, second paragraph.

Further, based on Appellant's understanding, the Examiner's basis for his rejection of claims 1-21 under 35 U.S.C. §112, second paragraph, is that the phrase "a single column having a width equal to a predetermined word-width" as recited in claim 1 and similarly in claims 8 and 16, is unclear to the Examiner. Appellant respectfully contends that this ground of rejection does not provide a basis for a rejection under 35 U.S.C. § 112, second paragraph. The purpose of a claim is not to explain technology or how it works. *S3 Inc. v. nVIDIA Corp.*, 59 U.S.P.Q.2d 1745, 1748 (Fed. Cir. 2001). The purpose is to state the legal boundaries of the patent grant. *Id.* Appellant respectfully asserts that the claimed subject matter in claims 1-21 can be determined by one having ordinary skill in the art. The rejection under 35 U.S.C. § 112, second paragraph, is not appropriate if the scope of the claimed subject matter can be determined by one having ordinary skill in the art. M.P.E.P. §2173. Consequently, Appellant respectfully asserts that claims 1-21 are allowable under 35 U.S.C. § 112, second paragraph.

B. Response to Examiner's assertion that Joffe discloses: "an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width" as recited in claim 1 and similarly in claim 16; "circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports" as recited in claim 1 and similarly in claim 16; and "a digital switch comprising: first and second ports for selectively coupling said first and second resources" as recited in claim 16, as discussed on pages 9-10 of Examiner's Answer.

The Examiner simply asserts that Joffe discloses the limitations cited in this heading without providing any basis in fact and/or technical reasoning for supporting such interpretations. For example, the Examiner asserts that Joffe discloses "an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width" as recited in claim 1 and similarly in claim 16, based on the phrase "all k-words of the burst are simultaneously transferred from the buffer and written to the shared memory on the k x m path" in Joffe. Examiner's Answer, page 9. However, the Examiner has not provided a basis in fact and/or technical reasoning to support the assertion that phrase "all k-words of the burst are simultaneously transferred from the buffer and written to the shared memory on the k x m path" can be interpreted as meaning an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width. The Examiner simply states "[s]ince this width takes up an entire row of a given row of the shared memory of Joffe, that memory may be considered a single column of that width." Examiner's Answer, page 9. This makes no logical sense. Again, the Examiner must provide a basis in fact and/or technical reasoning to support the assertion that the phrase "all k-words of the burst are simultaneously transferred from the buffer and written to the shared memory on the k x m path" in Joffe means an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that the phrase "all k-words of the burst are simultaneously transferred from the buffer and written to the shared memory on the k x m path" in Joffe means an array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided such objective evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claims 1 and 16. M.P.E.P. §2131.

Similarly, the Examiner must provide a basis in fact and/or technical reasoning to support the assertion that Joffe discloses: "circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports" as recited in claim 1 and similarly in claim 16; and "a digital switch comprising: first and second ports for selectively coupling said first and second resources" as recited in claim 16. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). Since the Examiner has not provided such objective evidence, the Examiner has not presented a *prima facie* case of anticipation in rejecting claims 1 and 16. M.P.E.P. §2131.

C. Response to Examiner's assertion that Joffe discloses the limitations of claims 2, 7 and 17, as discussed on page 10 of Examiner's Answer.

The Examiner asserts that Joffe discloses "a buffer associated with each port for converting words of data form an initial bit-width to said predetermined bit-width" as recited in claim 2 and similarly in claim 17. Examiner's Answer, page 10. The Examiner's basis for such an assertion is that Joffe allegedly converts the bit-width of m to the bit-width of k x m as shown in Figures 1 and 2. This does not make logical sense. Joffe discloses that during a transfer of data into the shared memory, a k word burst of m-bit words passes through a port. Column 2, lines 17-19. Joffe further discloses that during a prescribed time slot, all k-words of the burst are simultaneously transferred from the buffer and written to the shared memory on the k x m path. Column 2, lines 20-23. Joffe further discloses that during a transfer of data out of the shared memory, k words are read from the shared memory during another prescribed time slot and are transferred to a single memory access buffer. Column 2, lines 23-26. There is no language in Joffe that discloses "converting a bit-width of m to a bit-width of k x m" as alleged by the Examiner. Neither is there any language in Joffe that discloses a buffer associated with each port for converting words of data from an initial bit-width to the predetermined bit width. Thus, Joffe does not disclose all of the limitations of claims 2 and 17, and thus Joffe does not anticipate claims 2

and 17. M.P.E.P. §2131.

Further, as understood by Appellant, the Examiner asserts that Joffe discloses: "wherein said array comprises an array of random access memory cells of a read/write classification" as recited in claim 7; and "wherein data are exchanged through said ports as streams of data words of an initial word-width" as recited in claim 17. Examiner's Answer, page 10. However, the Examiner has not provided any basis in fact and/or technical reasoning to support such assertions. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that Joffe discloses the above-cited claim limitations. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that Joffe discloses the above-cited claim limitations, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 7 and 17. M.P.E.P. §2131.

D. Response to Examiner's assertion that Mathur discloses "circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports" as recited in claim 1 and similarly in claim 16, as discussed on page 11 of Examiner's Answer.

The Examiner had previously cited column 1, line 55 – column 2, line 11; column 4, lines 31-44; column 5, lines 56-61; column 11, lines 44-56 and Figures 6 and 7 of Mathur as disclosing "circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports" as recited in claim 1 and similarly in claim 16. Office Action (10/20/2006), page 5. The Examiner now cites column 3, line 66 –

column 4, line 2 of Mathur as disclosing the above-cited claim limitations. Examiner's Answer, page 11. Appellant respectfully traverses.

Mathur instead discloses that an internal data bus is coupled to the embedded packet memory. Column 3, lines 66-67. Mathur further discloses that it writes packets from the input ports to the embedded packet memory and reads the packets from the embedded packet memory to the output ports. Column 3, line 67 – column 4, line 2.

There is no language in the cited passage that discloses circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined-word width. Neither is there any language in the cited passage that discloses circuitry for writing selected data presented at the first one of the ports to a selected row in the array as a word of the predetermined-word width during a first time period. Neither is there any language in the cited passage that discloses reading the selected data as a word of the predetermined word-width. Neither is there any language in the cited passage that discloses reading the selected data as a word of the predetermined word-width from the selected row. Neither is there any language in the cited passage that discloses reading the selected data as a word of the predetermined word-width from the selected row during a second time period. Neither is there any language in the cited passage that discloses reading the selected data as a word of the predetermined word-width from the selected row during a second time period for output at the second one of the ports. Thus, Mathur does not disclose all of the limitations of claims 1 and 16, and thus claims 1 and 16 are not anticipated by Mathur. M.P.E.P. §2131.

E. Response to Examiner's assertion that Mathur discloses "a buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words" as recited in claim 8, as discussed on page 11 of Examiner's Answer.

The Examiner asserts that Mathur discloses "a buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words" as recited in claim 8. Examiner's Answer, page 11. The Examiner though has not provided any evidence to support the Examiner's assertion. The Examiner simply cites Figure 3 of Mathur. Examiner's Answer, page 11. However, there is no language in the description of Figure 3 or in the depiction of Figure 3 that discloses a buffer associated with each of the ports for assembling a stream of data words being input into the switch into a single word of a predetermined width and for converting single data words of the predetermined width being output from the switch into a stream of data words. The Examiner must provide evidence that shows that Mathur discloses each and every claim limitation. M.P.E.P. §2131. Since the Examiner has not provided such evidence, the Examiner has not established a *prima facie* case of anticipation rejecting claim 8. M.P.E.P. §2131.

F. Response to Examiner's assertion that Mathur discloses "a plurality of available address tables each for maintaining a queue of addresses available for writing said single words of data to a corresponding one of said banks; a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of said banks" as recited in claim 8, as discussed on pages 11-12 of Examiner's Answer.

As understood by Appellant, the Examiner asserts that Mathur discloses "a plurality of available address tables each for maintaining a queue of addresses available for writing said single words of data to a corresponding one of said banks; a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of said banks" as recited in claim 8. Examiner's Answer, page 11. The Examiner had previously cited column 9, lines 8-25 of Mathur as disclosing the above-cited claim limitations. Office Action (7/26/2006), page 3; Office Action (10/20/2006), page 6. The Examiner now cites Figures 6 and 7 of Mathur as disclosing the above-cited claim limitations. Examiner's Answer, pages 11-12. Appellant respectfully traverses.

If the Examiner is asserting that elements 60 and 80 in Figures 6 and 7, respectively, discloses the claimed plurality of address tables, Appellant respectfully traverses. There is no language in the description of Figures 6 and 7 that discloses that elements 60 and 80 are a plurality of available address tables each for maintaining a queue of addresses available for writing the single words of data to a corresponding one of the banks. Neither is there any language in the description of Figures 6 and 7 that discloses that elements 60 and 80 are a plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of the bank. Thus, Mathur does not disclose all of the limitations of claim 8, and thus claim 8 is not anticipated by Mathur. M.P.E.P. §2131.

G. Examiner asserts that Mathur discloses "a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width" as recited in claim 2 and similarly in claim 17, as discussed on page 12 of Examiner's Answer.

The Examiner asserts that Mathur discloses "a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width" as recited in claim 2 and similarly in claim 17. The Examiner previously cited column 6, lines 36-65 of Mathur as disclosing the above-cited claim limitation. Office Action (10/20/2006), page 5. The Examiner now cites column 6, lines 31-40 and Figure 6 of Mathur as disclosing the above-cited claim limitation. Examiner's Answer, page 12. Appellant respectfully traverses.

Mathur instead discloses that Figure 3 is a diagram of a switch chip with an internal packet memory showing more detail of port logic that send messages over an internal token bus. Column 3, lines 31-33. Mathur further discloses that port A logic 22 and port B logic 24 are bi-directional, each having a receive first-in-first-out FIFO 32 and a transmit FIFO 34 that connect to a twisted pair through physical-layer transceivers. Column 3, lines 33-36. Mathur additionally discloses that FIFOs 32, 34 are relatively small, their purpose is to hold data and provide a bus conversion between the external interface such as Media Independent Interface (MII) or RMII and the internal bus. Column 3, lines 36-40.

There is no language in the cited passage that discloses a buffer associated with each port. Neither is there any language in the cited passage that discloses a buffer associated with each port for converting words of data from an initial bit-width to the predetermined bit width. Thus, Mathur does not disclose all of the limitations of claims 2 and 17, and thus claims 2 and 17 are not anticipated by Mathur. M.P.E.P. §2131.

H. Response to Examiner's assertion that Mathur discloses "wherein each of said plurality of available address tables comprises a first-in-first-out memory" as recited in claim 10, as discussed on page 12 of Examiner's Answer.

The Examiner asserts that Mathur discloses "wherein each of said plurality of available address tables comprises a first-in-first-out memory" as recited in claim 10. Examiner's Answer, page 12. The Examiner had previously stated that the counter of Figure 6 operates by counting to the end of a packet. Office Action (7/26/2006), page 7; Office Action (10/20/2006), page 9. Appellant had previously stated that the Examiner must provide a basis in fact and/or technical reasoning to support the assertion that a counter of Figure 6 of Mathur discloses that each of the plurality of available address tables comprises a first-in-first-out memory. Appellant's Second Appeal Brief, pages 23-24. Apparently in response to Appellant's request for the Examiner to provide a basis in fact and/or technical reasoning to support the assertion that a counter of Figure 6 of Mathur discloses that each of the plurality of available address tables comprises a first-in-first-out memory, the Examiner asserts that the counters of Figures 6 and 7 "output[ting] from the table as a queue, which is the same as a FIFO operation." Examiner's Answer, page 12.

The Examiner has made a conclusion without providing any logical reasoning to support such a conclusion. That is, the Examiner is making conclusory statements without providing the logical steps to form such a conclusion. Hence, the Examiner has not provided any such objective evidence to support the assertion that Mathur discloses that each of the plurality of available address tables comprises a first-in-

first-out memory; and thus the Examiner has not presented a *prima facie* case of anticipation for rejecting claim 10. M.P.E.P. §2131.

I. Response to Examiner's assertion that Joffe teaches "wherein said initial bit-width is 48 bits and said predetermined word-width is 384 bits" as recited in claim 4, as discussed on pages 12-13 of Examiner's Answer.

The Examiner asserts that Joffe teaches "wherein said initial bit-width is 48 bits and said predetermined word-width is 384 bits" as recited in claim 4 based on the fact that Joffe uses variables m and k x m. Examiner's Answer, page 13. Appellant respectfully traverses. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that the teaching of the variables m and k x m in Joffe means having an initial bit-width of 48 bits and a predetermined word-width of 384 bits. *See Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that the teaching of the variables m and k x m in Joffe means having an initial bit-width of 48 bits and a predetermined word-width of 384 bits, and that it would be so recognized by persons of ordinary skill. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 4. M.P.E.P. §2143.

J. Other matters raised by the Examiner.

All other matters raised by the Examiner have been adequately addressed above and in Appellant's Second Appeal Brief and therefore will not be addressed herein for the sake of brevity.

II. CONCLUSION:

For the reasons stated above and in Appellant's Second Appeal Brief, Appellant respectfully asserts that the rejections of claims 1-21 are in error. Appellant respectfully requests reversal of the rejections and allowance of claims 1-21.

Respectfully submitted,

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